layer 3, as is known in the art for protecting underlying layers from moisture, contamination, etc.

The key steps of the invention begin with the deposition of a thick layer 5 of polyimide is deposited. A pattern 7 is exposed and etched through the polyimide layer 5 and the passivation layer 4 where the pattern 7 is the same as the pattern of the contact points 6. This opens the contact points 6 up to the surface 8 of the polyimide layer 5.

Electrical contact with the contact points 6 can now be established by filling the openings 7 with a conductor. The tops 9 of this metal conductor can now be used for connection of the IC to its environment, and for further integration into the surrounding electrical circuitry. Pads 10, 11 and 12 are formed on top of the top 9 of the metal conductors 7; these pads can be of any design in width and thickness to accommodate specific circuit design requirements. A larger size pad can, for instance, be used as a flip chip pad. A somewhat smaller in size pad can be used for power distribution or as a ground or signal bus. The following connections can, for instance, be made to the pads shown in Fig. 1: pad 10 can serve as a flip chip pad, pad 11 can serve as a flip chip pad or can be connected to electrical power or to electrical ground or to an electrical

signal bus, pad 12 can also serve as a flip chip pad. There is no connection between the size of the pads shown in Fig. 1 and the suggested possible electrical connections for which this pad can be used. Pad size and the standard rules and restrictions of electrical circuit design determine the electrical connections to which a given pad lends itself.

The following comments relate to the size and the number of the contact points 6, Fig. 1. Because these contact points 6 are located on top of a thin dielectric (layer 3, Fig. 1) the pad size cannot be too large since a large pad size brings with it a large capacitance. In addition, a large pad size will interfere with the routing capability of that layer of metal. It is therefore preferred to keep the size of the pad 6 small. The size of pad 6 is however also directly related with the aspect ratio of via 7. An aspect ratio of about 5 is acceptable for the consideration of via etching and via filling. Based on these considerations, the size of the contact pad 6 can be in the order of 0.5 um. to 3 um. the exact size being dependent on the thickness of layers 4 and 5.

The present invention does not impose a limitation on the number of contact pads that can be included in the design; this

number is dependent on package design requirements. Layer 4 in Fig. 1 can be a typical IC passivation layer.

The most frequently used passivation layer in the present state of the art is plasma enhanced CVD (PECVD) oxide and nitride. In creating layer 4, a layer of approximately 0.2 um. PECVD oxide is deposited first followed by a layer of approximately 0.7 um. nitride. Passivation layer 4 is very important because it protects the device wafer from moisture and foreign ion contamination. The positioning of this layer between the sub-micron process (of the integrated circuit) and the tens-micron process (of the interconnecting metalization structure) is of critical importance since it allows for a cheaper process that possibly has less stringent clean room requirements for the process of creating the interconnecting metalization structure.

Layer 5 is a thick polymer dielectric layer (for example polyimide) that have a thickness in excess of 2 um (after curing). The range of polyimide thickness can vary from 2 um. to 30 um. dependent on electrical design requirements.

For the deposition of layer 5 the Hitachi-Dupont polyimide HD 2732 or 2734 can, for example, be used. The polyimide can be spin-on coated and cured. After spin-on coating, the polyimide